Radiation Evaluation of a 0.18 µm Commercial CMOS Process and Modified Radiation Hardened Versions of this Process

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***Abstract*--We present radiation data, Total Ionizing Dose and Single Event Effects, on the LSI Logic's commercial 0.18 µm process and its radiation hardened version. Test results, are discussed in this paper. No Single Event Latch-up (SEL) was observed up to a LET of 75 MeVcm^2/mg for radiation hardened version, while the commercial process was very sensitive to SEL.**

I. INTRODUCTION

The use of commercial digital foundries with enhanced radiation tolerant processes could provide a savings in volume, power and weight versus other options for science and spacecraft designs. Albeit Field Programmable Gate Arrays (FPGA) are becoming of wider spread use, there are still a large number of applications that require Application Specific Integrated Circuits (ASIC) or structured ASIC for their lower Non-Recurring Engineering (NRE) cost and faster turn-around time in comparison to ASIC. It is therefore important to evaluate the radiation performance of CMOS digital foundries. This paper presents radiation evaluation data, total ionizing dose (TID) and single event effect (SEE), on LSI Logic commercial 0.18 µm process and two different radiation hardened versions of this process. The results are analyzed and discussed.

II. TESTED DEVICES AND EXPERIMENTAL TEST CONDITIONS

The tested standard process is a matured technology that has been in volume production for more than four years. It is a 0.18 µm drawn bulk process with Shallow Trench Isolation (STI). The core voltage is 1.8V. The technology supports I/O voltages up to 3.3V and up to 6 metal layers with low K inter metal dielectrics material. The gate oxide thickness is 3.4 nm and the STI thickness is 300 nm. Up to 16 million logic gates can be used on a chip.

Two manufacturer's test vehicles are used. First one is a 512 Kbit SRAM memory chip. The minimum cycle time is about 50 ns, and the power supply voltage is 1.8V. The SRAM test chip is packaged in a 64 bit ceramic PGA package. The second test vehicle is a logic chip that contains 64 64-bit arithmetic logic units (ALU). This chip has been designed with full scan methodology. There are 4 scan chains with a length of 3072 flip-flops each. This design was synthesized to operate at a maximum speed of 20 MHz. The I/O buffers used in this design consist of 3 voltage types: 1.8V, 2.5V, and 3.3V. The logic test chip is packaged in a 313 pin plastic EPBGA.

TID irradiations were performed on SRAM test vehicle with NASA-GSFC Co-60 source. Parts were irradiated up to the total dose level of about 300 krad-Si at a dose rate ranging from 1 to 10 krad-Si per hour. After irradiation parts were submitted to a one-week annealing at room temperature. 5 parts were irradiated with static on mode and 2 parts were irradiated without bias. No pattern was loaded before irradiation in the memory devices with static on mode bias. In addition to a full functional testing, the three different device standby power supply currents, periphery, I/O, and memory core, were measured before irradiation and after each irradiation step.

SEE tests were performed at the TEXAS A&M cyclotron with 15 MeV per nucleon heavy ion beams. Additional high energy SEE testing was performed on the SRAM test vehicle at Michigan State University (MSU) [1] with a 131 MeV/u Xenon beam. Laser tests were also performed at the Naval Research Laboratory (NRL) laser test facility [2].

The SRAM test vehicle was tested with a specific set-up developed at NASA-GSFC. Two different test modes were investigated:

- Static test: a test pattern is loaded in the device under test (DUT) before irradiation, and then checked after the irradiation.
- Dynamic test: a test pattern is loaded in the DUT before irradiation. During irradiation the DUT is continuously read.

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For both test modes the detected errors were recorded for further analysis. Four different test patterns were tested: all 0, all 1, checkerboard, and reverse checkerboard.

The logic test chip was tested with a specific test set-up developed at NASA-GSFC. Two different test modes were investigated:

- ALU mode: In this mode 48 of the device 64 ALUs are operated in sequence one after each other. A static input is applied, and each ALU tested performs in sequence all 16 binary and 16 logical arithmetic operations. The test principle is the golden chip test method. The outputs of the DUT are compared to those of a reference device operated under the same conditions. In this mode, only one ALU is tested at a time. The number of tested bits is 128 bits (input flip-flops) 25% of the time and 64 bits (output flip-flops) 25% of the time.
- Scan chain mode: in this mode we use the logic test chip scan chain capability. All flip-flops of each of the four ALUs blocks are chained together to form a 3072 bits shift register. We have connected three 3072 bits shift registers to form a 9216 bits shift register. The input signal alternates 1 and 0 at each clock cycle. The number of tested bits in this mode is 9216.

For both test vehicles, the power supply currents of the DUT were monitored and charted during irradiation to detect the occurrence of SEL or other anomalous conditions. In case of SEL, the DUT power supplies are shutdown.

III. TEST RESULTS ON STANDARD PROCESS

A. *Total ionizing dose results*

TID test results on the SRAM test vehicle indicate that all the parts stay functional up to the maximum dose level of about 300 krad-Si. The unbiased parts showed little degradation after 300 krad-Si. For the parts that were biased during irradiation, no significant degradation of the measured electrical parameters was observed up to a dose level of 90 krad-Si. The I/O and periphery power supply currents show little degradation after 300 krad-Si. However, the memory core power supply current is extremely degraded after 300 krad-Si. Fig. 1 shows the degradation versus total dose of the memory core power supply current when the memory is loaded with an all 1 pattern. The all 1 pattern is the pattern for which the largest degradation was observed. This seems to indicate that when the parts are biased, the preferential value of most memory cells is 0. Post irradiation room temperature annealing data show a significant but not complete recovery.

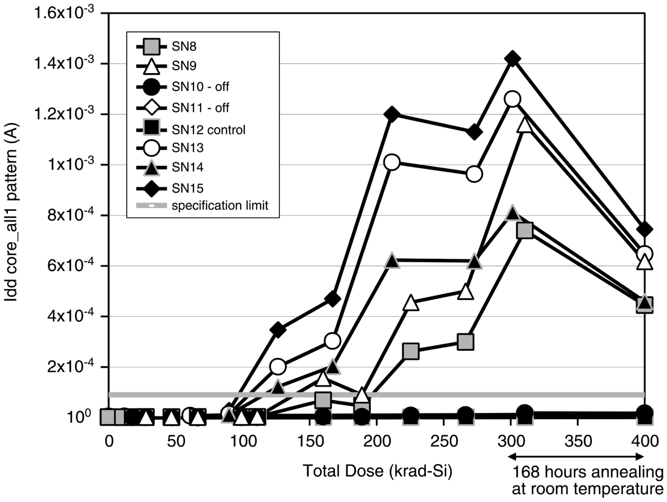

Fig. 1. Degradation versus total dose of memory core power supply standby current

B. *Single Event Effect Test Results*

Fig. 2 shows the SEL and Single Event Upset (SEU) cross-sections curves for the SRAM test vehicle. Test results show SEL sensitivity at LET higher than 29 MeVcm^2/mg. Laser testing at NRL showed that the SEL did not occur in the memory core but in the periphery area of the device. The maximum measured latch-up current was 180 mA for a nominal current of less than 1 mA. Only limited SEU testing was possible because of the SEL sensitivity. As the different test modes and test patterns, did not show any significant effect on SEU sensitivity, fig. 2 shows an average of test results for all different test conditions. We can see in fig. 2 that at the lowest LET of 2.8 MeVcm^2/mg the cross-section has not decreased significantly. This indicates a LET threshold well below this value. We can also see that the SEU cross-section increases slightly with LET. The maximum measured SEU cross-section is about 3 10^{-8} cm^2/bit. An analysis of test data shows that the number of Multiple Event Upsets (MEU) at LET up to 14 MeVcm^2/mg is negligible. However, MSU run data at a LET of 41 MeVcm^2/mg (14 MeVcm^2/mg with 70 degrees tilt), show about 44% of MEU. All MEU are double bit errors in two neighboring cells. We believe that it is due to a higher diffusion at higher LET, which leads to a higher cross-section.

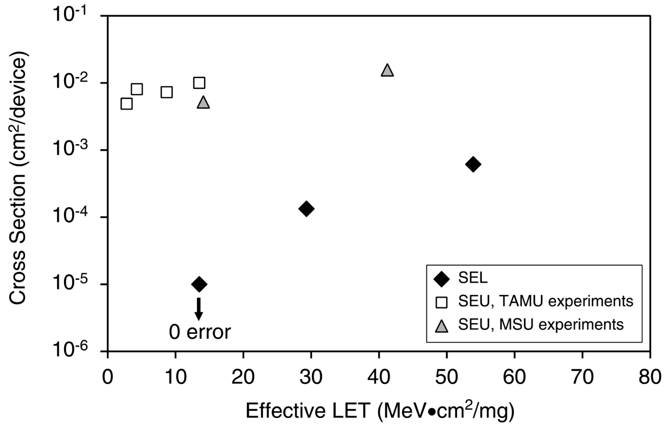

Fig. 2. SRAM test vehicle, standard process, SEU and SEL cross-section curves

Test results show an extremely high sensitivity to micro latch-up of Logic test chip at LET higher than 8 MeVcm^2/mg. During heavy ion testing the effect manifests itself by a burst of errors, but no large enough current increase to trigger the latch-up detection. Laser testing confirmed the micro latch-up assumptions with sensitive areas spread all over the die. Fig. 3 shows the evolution of 1.8V power supply current when 3 sensitive locations are hit successively. At the first location the current jumped from its nominal value of 16 mA to 66 mA. The current reached a 106 mA value at the third location. Because of this extremely high micro latch-up sensitivity, SEU testing was only possible at the lowest LET of 2.8 MeVcm^2/mg. The measured cross-section at LET 2.8 MeVcm^2/mg is about 1.12 10^{-9} cm^2/bit.

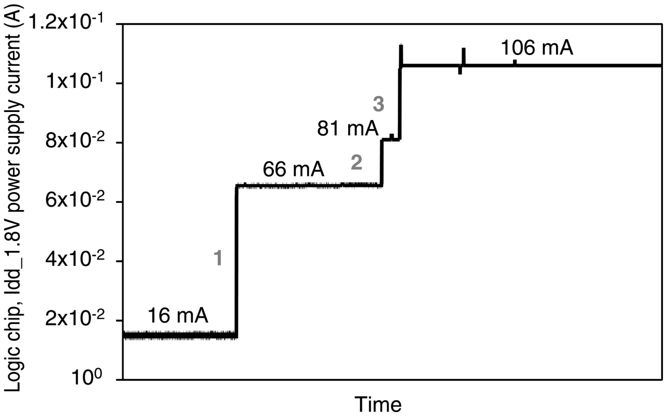

Fig. 3. Logic test vehicle, 1.8V supply current evolution when sensitive locations are hit with the laser.

IV. TEST RESULTS ON ENHANCED PROCESSES

A. *Introduction*

To decrease the SEL sensitivity of the CMOS bulk process, the manufacturer developed two different versions of a modified bulk process with a buried layer. The main difference between the two versions is the doping level of the buried layer. Test samples of each modified process, dose A and dose B, were provided for both test vehicles. Only SEE tests were performed on modified bulk process.

B. *Tests results on modified bulk processes*

Both modified bulk processes are not sensitive to SEL up to the maximum tested LET of 75 MeVcm^2/mg. Fig. 4 shows the SEU cross section curve for the SRAM test vehicle for bulk and modified bulk processes. We cannot see any significant difference between the two modified processes. We can see that at high LET the cross sections of both modified bulk processes continue to increase with LET. The maximum measured cross-section is about 2.8 10^{-7} cm^2/bit to compare to a cell area of about 5.58 10^{-8} cm^2. This points to a diffusion process where a single particle causes multiple upsets. Data analysis showed that at high LET more than 35% of events are multiple events where 2 or 3 neighboring cells are upset. This is a little bit less than the number of MEU observed on the bulk process.

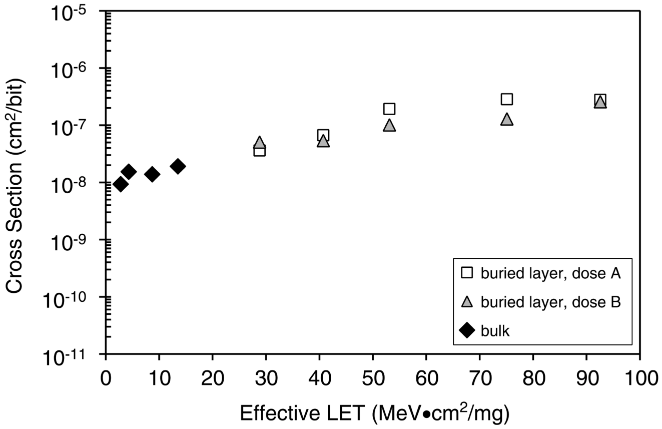

Fig. 4. SEU cross section, SRAM test vehicle, radiation enhanced processes

Fig. 5 shows a picture of the SEU cross-section of the logic test vehicle. Here again, we cannot see a significant difference the two hardened processes, and a we also see a slight increase of cross-section with LET. The maximum measured cross-section is about 10^{-6} cm^2/flip-flop. We explain the higher sensitivity of the shift register test because of a higher test speed for shift register tests (5 MHz) than for ALU test (1.25 MHz).

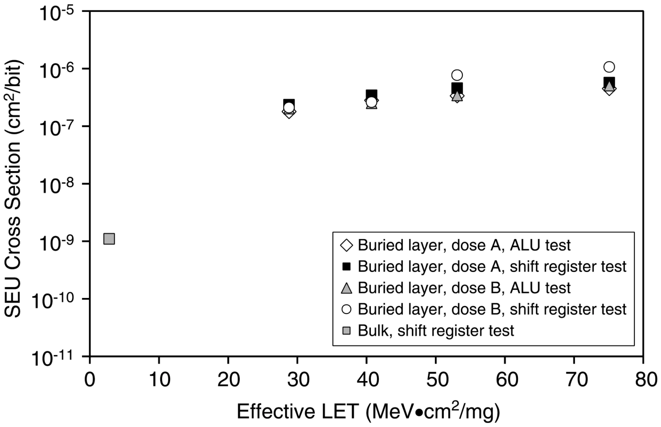

Fig. 5. SEU cross-section, logic test vehicle

V. CONCLUSIONS

As expected, for a 0.18 µm CMOS process, the TID tolerance is good. No noticeable degradation is observed up to a total dose of 90 krad-Si. SEE test results show that the commercial bulk process is very sensitive to SEL. Modified bulk process exhibits significant improvement in SEL tolerance. No SEL was observed up to a LET of 75 MeVcm^2/mg. The SEU sensitivity is high as expected. The LET threshold is lower than 2.8 MeVcm^2/mg and the maximum measured cross section of about 2 10^{-7} cm^2/bit for a SRAM cell and 10^{-6} cm^2/bit for a flip-flop. However, the multiple events observed in the SRAM test vehicle only affect 2 or 3 neighboring cells and can be easily mitigated with standard error and detection codes. Based on low LET threshold, both SRAM cells and flip-flops are expected to be sensitive to proton induced SEU as well. LSI Logic's modified 0.18µm process will satisfy most space projects requirements with adequate SEU mitigation.

VI. ACKNOWLEDGMENT

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VII. REFERENCES

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